FIG. 1

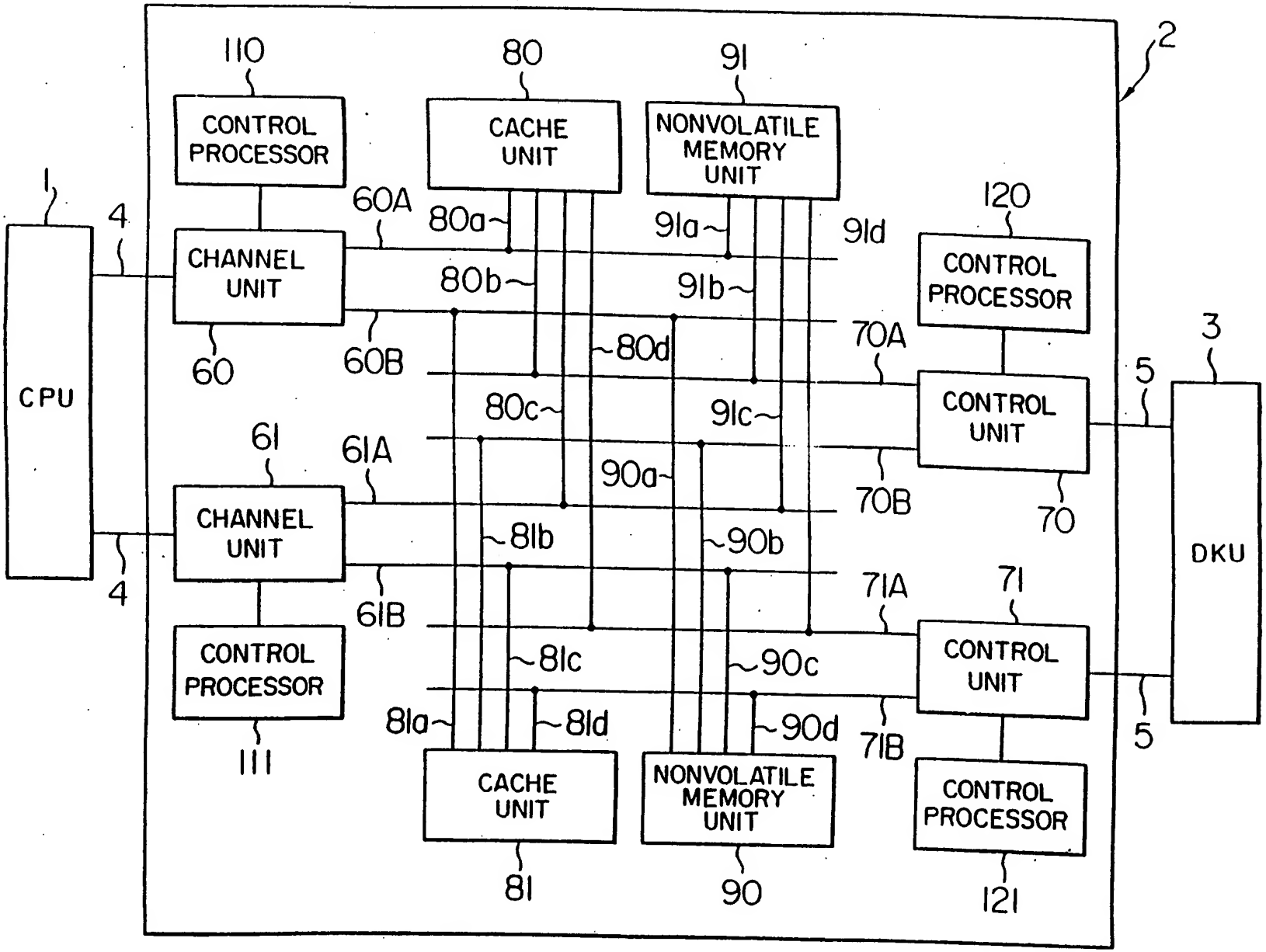

110
80
91
2
CONTROL PROCESSOR
CACHE UNIT
NONVOLATILE MEMORY UNIT
1
4
60A
80a
91a
91d
120
CONTROL PROCESSOR
CHANNEL UNIT
80b
91b
70A
3
CPU
60
60B
80d
5
DKU
80c
91c
61
61A
CONTROL UNIT
90a
70B
CHANNEL UNIT
81b
90b
70
4
71A
71
61B
CONTROL PROCESSOR
81c
90c
CONTROL UNIT
81a
81d
90d
71B
5
CACHE UNIT
NONVOLATILE MEMORY UNIT
CONTROL PROCESSOR
111
81
90
121

FIG. 2

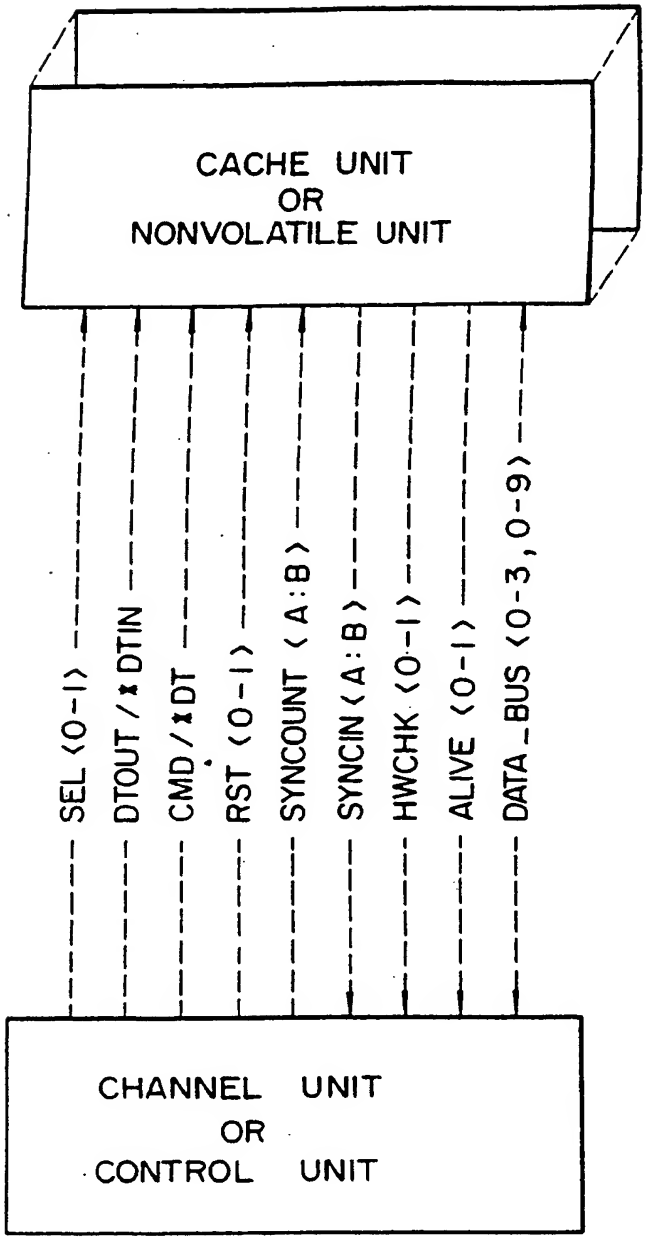

CACHE UNIT
OR
NONVOLATILE UNIT
SEL ⟨0-1⟩
DTOUT / ‡DTIN
CMD / ‡DT
RST ⟨0-1⟩
SYNCOUNT ⟨A:B⟩
SYNCIN ⟨A:B⟩
HWCHK ⟨0-1⟩
ALIVE ⟨0-1⟩
DATA_BUS ⟨0-3, 0-9⟩
CHANNEL UNIT
OR
CONTROL UNIT

FIG. 3

DATA BUS PROTOCOL

FIG. 4

DATA BUS MODE

DUOUT / ẋDTIN	CMD / ẋDT	BUS MODE
1	1	TRANSFER COMMAND
1	0	TRANSFER WRITE DATA
0	1	TRANSFER STATUS
0	0	TRANSFER READ DATA

FIG. 5

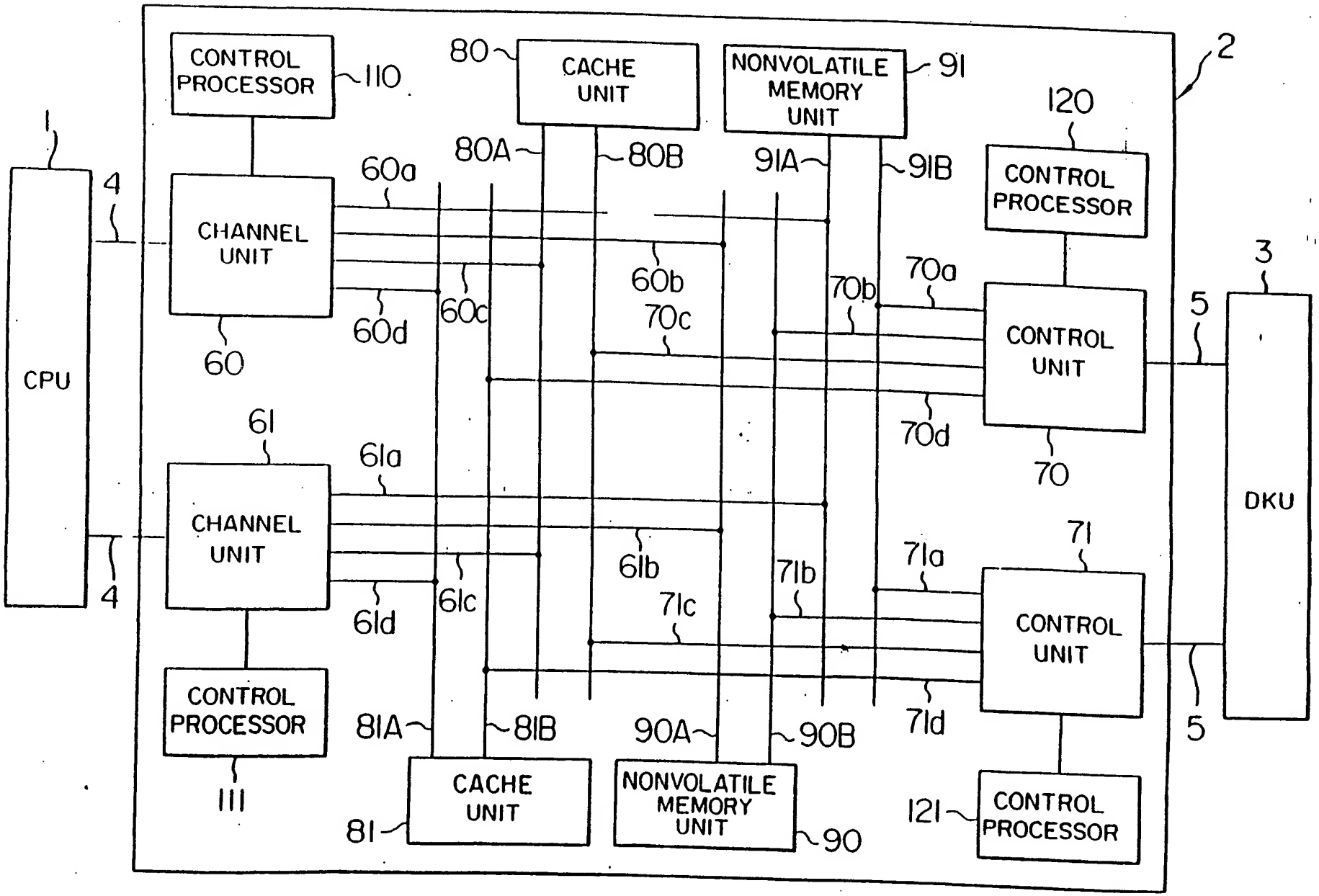

CONTROL PROCESSOR
110
80
CACHE UNIT
NONVOLATILE MEMORY UNIT
91
2
120
1
4
CHANNEL UNIT
60a
80A
80B
91A
91B
CONTROL PROCESSOR
60b
70a
70b
3
60c
70c
60d
5
CPU
60
CONTROL UNIT
DKU
61
61a
70d
70
CHANNEL UNIT
61b
71
71a
71b
61c
71c
61d
CONTROL UNIT
CONTROL PROCESSOR
81A
81B
90A
90B
71d
5
111
CACHE UNIT
NONVOLATILE MEMORY UNIT
121
CONTROL PROCESSOR
81
90

FIG. 6

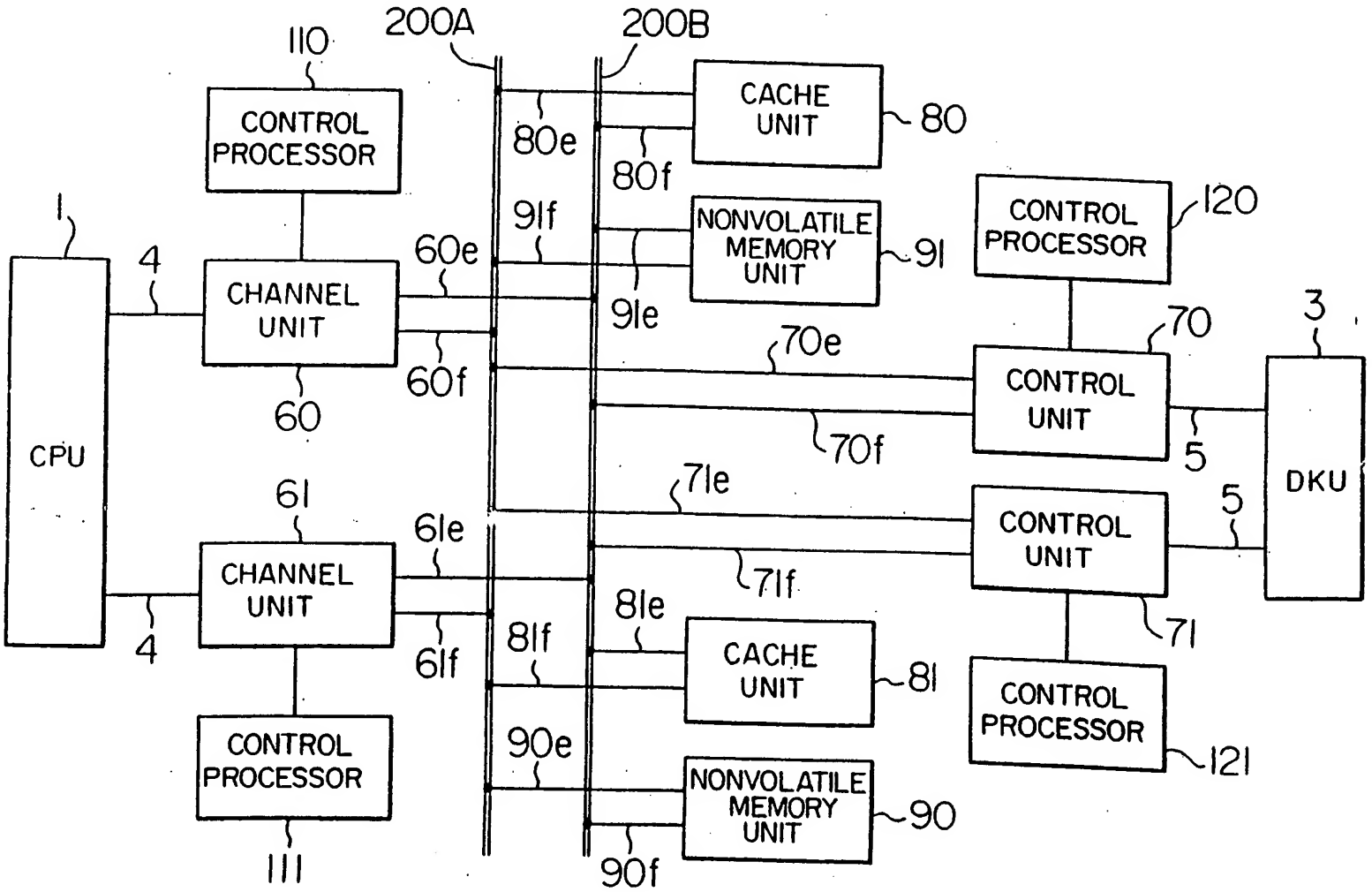
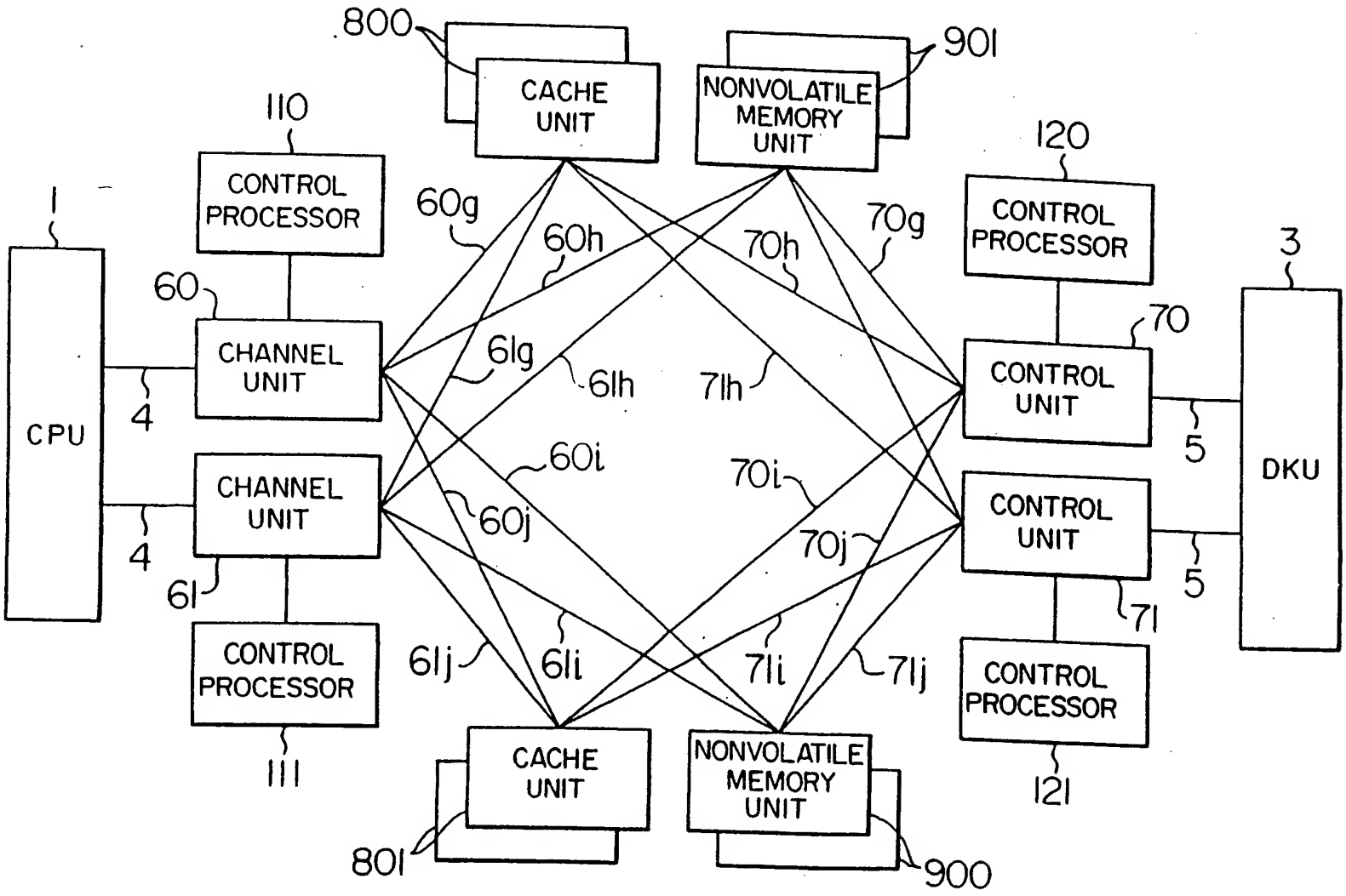

110
200A
200B
CONTROL PROCESSOR
CACHE UNIT
80
80e
80f
1
4
CHANNEL UNIT
60e
91f
NONVOLATILE MEMORY UNIT
91
91e
120
CONTROL PROCESSOR
3
70
60f
70e
CONTROL UNIT
60
70f
CPU
5
DKU
61
71e
61e
CONTROL UNIT
5
CHANNEL UNIT
71f
71
81e
4
61f
81f
CACHE UNIT
81
CONTROL PROCESSOR
90e
121
NONVOLATILE MEMORY UNIT
90
111
90f

FIG. 7


800
CACHE UNIT
901
NONVOLATILE MEMORY UNIT
110
CONTROL PROCESSOR
120
CONTROL PROCESSOR
1
CPU
60g
60h
70h
70g
3
60
CHANNEL UNIT
61g
61h
71h
70
CONTROL UNIT
4
5
DKU
60i
70i
CHANNEL UNIT
60j
70j
CONTROL UNIT
4
5
61
71
CONTROL PROCESSOR
61j
61i
71i
71j
CONTROL PROCESSOR
111
121
CACHE UNIT
NONVOLATILE MEMORY UNIT
801
900